THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 52

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RICHARD W. CUTTS, JR.,
KENNETH C. DEBACKER, ROBERT W. HORST,
NIKHIL A. MEHTA, DOUGLAS E. JEWETT,
JOHN D. ALLISON, and RICHARD A. SOUTHWORTH

Appeal No. 96-0905
Application 08/116,950[1]

ON BRIEF

Before KRASS, FLEMING, and CARMICHAEL, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

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[1]Application for patent filed September 7, 1993. According to appellants, this application is a continuation of Application 07/517,533, filed April 25, 1990; which is a continuation of Application 07/282,538, filed December 9, 1988.

This is a decision on appeal from the final rejection of claims 1 through 8, 11 through 14 and 16 through 26, all of the claims remaining in the application.

The invention is directed to a fault-tolerant computer system employing multiple CPUs. Each CPU has its own independent clock in order to avoid imposing the expense, complexity and timing problems of typical fault-tolerant clocking. However, the CPUs are loosely synchronized by detecting certain events and stalling any CPU ahead of the others until all the CPUs execute the required function simultaneously. Interrupts are also synchronized to the CPUs in order that the CPUs all execute the interrupt at the same point in the instruction stream which they are all executing. More particularly, each of the CPUs has a counter which counts machine cycles corresponding to execution cycles but does not count stall cycles. Further, each CPU is interrupted at some predetermined count value. All interrupts are made to occur at the same virtual time in each CPU, though not necessarily at the same point in real time.

Representative independent claim 1 is reproduced as follows:

1. A multiple CPU system, comprising:

a) a plurality of CPUs concurrently executing a same instruction stream, the CPUs each being clocked independently of one another to provide separate machine

clock cycles for each CPU, so that said instruction stream is executed asynchronously over plural instructions and any of said CPUs may be leading other of said CPUs, said machine clock cycles including execution cycles where an instruction of said instruction stream is executed and stall cycles where an instruction of said instruction stream is not executed, each CPU having a memory request input/output port;

b) a common memory coupled to the input/output ports of said CPUs, the common memory implementing a memory request only after receiving identical requests from all of said CPUs, the memory sending an acknowledge signal to the CPUs when implementing a memory request, each of the CPUs executing stall cycles while awaiting implementation of a memory request by the common memory as signalled [sic, signaled] by said acknowledge signal;

c) each of the CPUs having a counter to count machine clock cycles corresponding to execution cycles but which is inhibited from counting machine clock cycles corresponding to stall cycles; and

d) said CPUs having an interrupt circuit responsive to an external interrupt request occurring at any time unsynchronized with said execution of said instruction stream, said interrupt circuit being coupled to said counters in said CPUs and responsive to a selected count in each of said counters for separately interrupting each CPU at an identical instruction execution cycle, any one of the CPUs which may be leading being interrupted first while other of said CPUs continue to execute instructions so that if said CPUs are executing different instructions in said stream then said CPUs may be interrupted at different instants in real time.

The examiner relies on the following references:

Kreis et al. (Kreis)	3,921,149	Nov. 18, 1975
Kolb et al. (Kolb) (PCT)	WO 85/02698	Jun. 20, 1985

Claims 1 through 8, 11 through 14 and 16 through 26 stand rejected under 35 U.S.C. § 103 as unpatentable over Kolb in view of Kreis.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

At the outset, we note that, in accordance with appellants' statement at page 6 of the principal brief, independent claims 1, 3, 5, 7 and 23 will stand or fall together, and dependent claims 12, 13, 18, 20, 21 and 26 will stand or fall together. Appellants separately argue the merits of dependent claims 12, 13, 18, 20, 21 and 26 at page 12 of the principal brief and throughout the briefs, arguing that the instant invention's interrupt only on a selected value registered by the counters distinguishes over the applied references. However, dependent claims 2, 4, 6, 8, 11, 14, 16, 17, 19, 22, 24 and 25 will stand or fall with the claims from which they depend since appellants make no separate argument with regard to the specific limitations added by these claims, i.e., with regard to the common memory modules and local memories not accessible to other CPUs.

We also note that while Kreis is applied by the examiner for the teaching of access requests to a common memory which are

voted, there is no argument by appellants regarding such a limitation or teaching by Kreis. With regard to Kreis, appellants argue only that the reference does not provide for the alleged deficiencies of Kolb. Accordingly, for purposes of this appeal, we will focus, as do appellants and the examiner, on the teachings of Kolb.

With regard to the independent claims, the examiner recognizes that Kolb does not specifically teach that the CPU cycle counters count machine cycles corresponding to execution cycles but not machine cycles corresponding to stall cycles. However, the examiner points to various portions of Kolb (page 3, line 33 to page 4, line 1; page 9, lines 17-35) indicating that there are many alternative possible choices of processor events which can be used as a virtual time tick for the purpose of measuring virtual time. Therefore, the examiner concludes, and we agree, that it would have been obvious to have counted machine cycles corresponding to execution, but not stall, cycles in order to measure virtual time.

In response to appellants' argument that all the claims require also that the interrupt signal is to be applied at a "selected" or a "preselected" count value, the examiner points out that in the second embodiment of Kolb, when an interrupt

signal is received by the lead processor, the location of the processor in the program is stored and the lead processor continues on after servicing the interrupt. Then, when a lagging processor advances to the same position in the program, it is also notified of the interrupt so that the interrupt is serviced at the same virtual time by both processors. Accordingly, the examiner considers the stored virtual time in Kolb as the claimed "selected" or "preselected" count.

In response, appellants contend that even if the examiner's position, i.e., that the virtual time used to interrupt the lagging processors in Kolb is equivalent to the preselected/selected count of the instant independent claims, the instant claims still distinguish over Kolb because they require that "each" of the CPUs contains the recited interrupt circuit and is interrupted at the preselected/selected count so that "each" of the CPUs must be interrupted in accordance with the preselected/selected count. Yet, the lead processor of Kolb receives the first interrupt as soon as it is sent at some "random" virtual time, and not at the preselected/selected time recited in the instant claims.

We will sustain the rejection of claims 1 through 8, 11 through 14 and 16 through 26 under 35 U.S.C. § 103 because while

we agree with appellants' last argument that the lead processor of Kolb receives the interrupt request and executes it as soon as it is sent at some random virtual time, and not at a preselected/selected time, the instant claims are not so limiting as to distinguish over Kolb in this regard. Since the claims are open-ended, i.e., the multiple CPU system "comprising"..., the "plurality" of CPUs recited in the claims need not include the lead processor as in Kolb but may very well include all of the processors of Kolb but for the lead processor.

We find the examiner's approach of interpreting the virtual time used to interrupt the lagging processors in Kolb as a "preselected" or "selected" count to be sound. We also find that each of the independent claims, in one form or another, requires that each of the CPUs has an interrupt circuit[2] and a counter and that the interrupt circuit is responsive to an external interrupt

[2]While the language of claim 1 ("said CPUs having an interrupt circuit") and claim 3 ("an interrupt circuit connected to all of said CPUs") might, at first glance, be interpreted as permitting a single, separate interrupt circuit coupled to each of the CPUs, it is clear from the disclosure, e.g., page 17, line 25 and Figure 2, that each of the CPUs has an interrupt circuit 65. This, coupled with appellants' similar interpretation, or admission, at page 5, fourth line up from the bottom, of the reply brief, that the language of the claims mean that "each of the CPUs contains the recited interrupt circuit" would make any other interpretation unreasonable, in our view.

request occurring at any time. It is also required that the interrupt circuit and counter be coupled so that the interrupt circuit is also responsive to a selected, or preselected, count in the counter for separately interrupting each CPU at an identical instruction execution cycle. Accordingly, even the CPU which may be leading is also subject to the selected, or preselected, count determining when that CPU will be interrupted. In Kolb's system, specifically the second embodiment relied on by the examiner, the lead processor appears to receive the interrupt request immediately and to service that interrupt at any random time the interrupt request is made. The lead processor then proceeds in the program although the specific location in the program at the time of the interrupt is stored so as to be used by the lagging processors in order to interrupt at the same virtual time within the program. Therefore, as appellants' argument goes, since the instant claims require that each of the CPUs must be interrupted in accordance with the preselected, or selected, count and Kolb's leading processor is clearly not interrupted in accordance with such a count, nor is there any evidence as to why it would have been obvious to modify Kolb in any manner to achieve such (and Kreis adds nothing in regard to

remedying this deficiency in Kolb), the instant rejection under 35 U.S.C. § 103 should not be sustained.

We would not sustain the rejection under 35 U.S.C. § 103 if interpretation of the instant claims required that the leading CPU, as disclosed by Kolb, be part of the claimed "plurality of CPUs." However, since the instant claims are open-ended, because of the "comprising" recitation, it is a fair interpretation to read the instant claims on the disclosure of Kolb with the consideration that all of Kolb's CPUs, other than the lead processor, comprise the claimed "plurality of CPUs." Then, of course, after the "preselected" count is established by the lead processor upon randomly receiving the interrupt request and storing the specific location in the program at the time of the interrupt, all of the other CPUs, i.e., those belonging to the claimed "plurality of CPUs," will be subject to being interrupted "responsive to a selected count...for separately interrupting each CPU at an identical instruction execution cycle." The way appellants' "multiple CPU system" is set forth in the instant claims, it allows for extra CPUs (e.g., Kolb's lead processor) not part of the claimed "plurality of CPUs" and, therefore, not subject to the specific limitations laid out for each of the "plurality of CPUs" in the claims.

It is our view that if appellants' claims, in some way, required that *all* of the CPUs in the multiple CPU system were subject to the claimed requirements regarding interruption responsive to a preselected count, this would distinguish over the applied references for the reasons set forth in the reply brief. However, as presently claimed, we agree with the examiner's rejection of claims 1 through 8, 11 through 14 and 16 through 26 under 35 U.S.C. § 103.

The examiner's decision is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED

Errol A. Krass Administrative Patent Judge	)	
Michael R. Fleming Administrative Patent Judge	)	BOARD OF PATENT APPEALS AND INTERFERENCES
James T. Carmichael Administrative Patent Judge	)	

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